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A Programmable CMOS Delay Line for Wide Delay Range Generation and Duty-Cycle Adjustability

Bilal I. Abdulrazzaq[1,2]*, Izhal Abdul Halin[1], Lee Lini[3], Roslina M. Sidek[1] and Nurul Amziah Md. Yunus[1]

[1]Department of Electrical and Electronic Engineering, Faculty of Engineering, Universiti Putra Malaysia, 43400 UPM Serdang, Selangor, Malaysia
[2]Department of Electronic and Communications Engineering, Al-Nahrain University, Al-Jadriya Complex, Baghdad 10070, Iraq
[3]Faculty of Engineering, Multimedia University, Persiaran Multimedia, 63100 Cyberjaya, Malaysia

ABSTRACT

A programmable CMOS delay line circuit with microsecond delay range and adjustable duty cycle is proposed. Through circuit simulation, approximately 2μs delay range can be achieved using 10-bit counter operating at a clock frequency of 500MHz. Utilising synchronous counters instead of synchronous latches has significantly reduced the large occupied active silicon area as well as the huge power consumption. The generated coarse time delay has shown excellent linearity and immunity to PVT variations. The proposed CMOS delay line is designed using a standard 0.13μm Silterra CMOS technology. The active layout area is (101 x 142) μm^2, and the total power consumption is only 0.1 μW.

Keywords: CMOS delay line, synchronous counter, latches, delay element, delay range, duty cycle, linearity, PVT variations

INTRODUCTION

Recently, CMOS delay lines have gained increasing interest because of the growing needs for specialised time management circuits (Murakami & Kuwabara, 1991). For example, in microprocessors, the programmable delay line which is situated between the microprocessor and its memory is used to ensure perfect synchronisation of clock signals/data packets at both the transmitting and receiving ends. In Time-of-Flight (ToF) range-finding systems, a delay

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E-mail addresses:
bilal.i.abdulrazzaq@gmail.com (Bilal I. Abdulrazzaq),
izhal@upm.edu.my (Izhal Abdul Halin),
linilee@mmu.edu.my (Lee Lini),
roslina@upm.edu.my (Roslina M. Sidek),
amziah@upm.edu.my (Nurul Amziah Md. Yunus)
*Corresponding Author

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line is used to delay the light signal emitted from the sensor in order to mimic objects at different distances during ToF sensor characterisation (Halin et al., 2011; Kawahito et al., 2007). In time-dependent image sensors, the experimental setup for imaging uses an external delay line for shifting the imaging window. However, it is desirable to integrate the delay line as part of the image sensor system (Kawahito et al., 2013). Moreover, many CMOS delay line circuits play a substantial role in many sub-systems of Time-Interval Measurement (TIM) circuits such as Time-to-Digital Converters (TDCs) and Digital-to-Time Converters (DTCs) for digitization of short-time intervals (Andreani, Bigongiari, Roncella, Saletti, & Terreni, 1999; Rahkonen & Kostamovaara, 1993). In all of these applications, programmable wide delay ranges are required for proper operation in order to avoid functionality failure of the system.

On the other hand, obtaining an output digital signal with adjustable pulse-width feature is becoming a significant demand by many VLSI systems. This is attributed to two main reasons. First, different applications of these VLSI systems require different duty cycles of the input signals (Murakami & Kuwabara, 1991). Second, the heavy capacitive load of these VLSI systems needs an efficient digital driving circuitry. This driving circuitry is required to maintain the duty cycle of the output signal within acceptable boundaries (Kao, Cheng, & You, 2015).

Attaining both programmable wide delay range and adjustable duty cycle can be achieved by a delay line circuit in which these two functions are integrated. Accordingly, many designs found in the literature have been proposed. Conventional wide-range delay lines use N numbers of synchronous latches (D flip-flop) as their delay element with each latch having a delay unit of τ (s) which is equal to 1 clock cycle. Only one of these latches is tapped at a desired node to generate the delay. For example, to generate a 1µs delay, this type of delay line would require 1000 latches operating at 1GHz. The circuit topology for 1000 latches would be excessively large on silicon. Moreover, power dissipation would also be high due to the clocking of a large number of latches (Jovanovic & Stojcev, 2009). Another example is the DS1124 8-bit programmable delay line which uses tapped-delay line architecture. This architecture is implemented using an array of buffers connected to a single output line via a network of switches. For example, the buffer-based tapped delay line works on the principle that propagation delay time is added as the number of buffers in a signal line is increased. The DS1124 delay line offers a maximum delay of 64ns (Products, 2009). Although the aforementioned architecture is useful for implementing large maximum delays, they lack for the adjustable duty-cycle feature. Alternatively, the design proposed by (Murakami & Kuwabara, 1991) offers both programmable delay range and adjustable duty cycle. However, the achievable maximum delay range is only 20ns, making this architecture non-feasible for many high-performance applications.

In order to fill this research gap, this paper presents a new CMOS coarse delay line architecture which can generate both programmable microsecond delay range and adjustable microsecond duty-cycle control. The new architecture proposes the use of a synchronous counter to generate wide delay ranges, instead of a large number of latches. Thus, power consumption is significantly reduced and the occupied area is also minimised. The remainder of the paper is organised as follows. The next section presents the architecture of the proposed CMOS coarse delay line circuit before discussing the results and discussions. The last section summarises and concludes this paper.

PROPOSED ARCHITECTURE

The proposed architecture of the coarse CMOS delay line is shown in Figure 1.

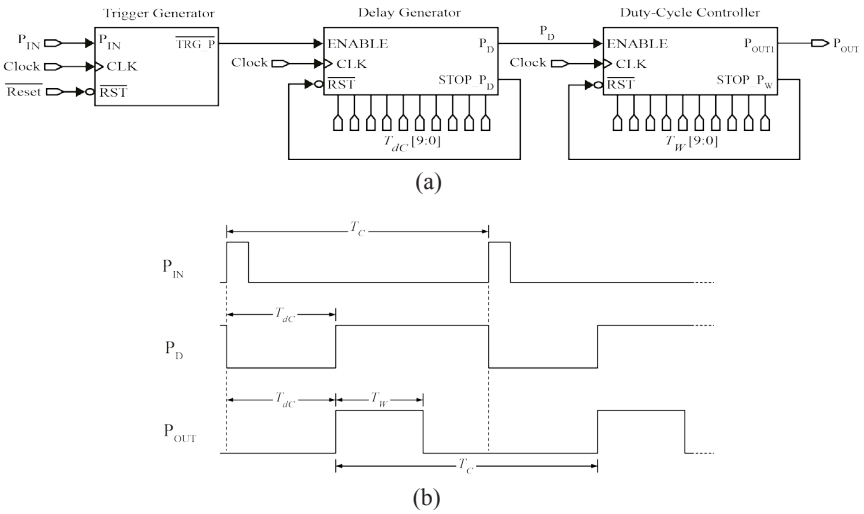


Figure 1. Simplified CMOS coarse delay line: (a) block diagram; (b) timing diagram

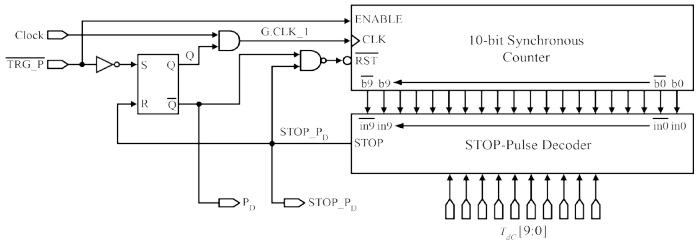
Figure 1 (a) shows the proposed architecture consists of three main blocks, namely Trigger Generator, Delay Generator, and Duty-Cycle Controller. Each circuit block performs one main function. To explain this, a simplified timing diagram illustrating the functionality of the three blocks is shown in Figure 1(b). The input periodic signal triggers the first circuit block which is input-pulse Trigger Generator circuit. This Trigger Generator detects the leading edge of the input signal P_{IN} which has a period T_C. Thereafter, the Delay Generator produces an output signal, P_D, which is used to enable/disable the Duty-Cycle Controller circuit. The disable period is T_{dC} which is the programmable generated coarse time delay, and the enable period is $T_C - T_{dC}$. Finally, during $T_C - T_{dC}$ period, the Duty-Cycle/pulse-width Controller circuit produces an output signal, P_{out}, whose programmable generated pulse-width is T_W and period is T_C.

The programmable duty-cycle delayed output pulses are achieved using START and STOP pulses. A detailed description of the building blocks in Figure 1 (a) are given below.

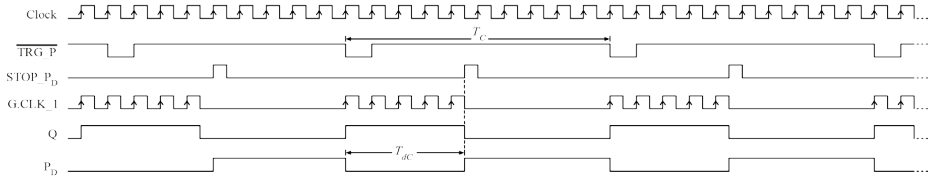
Delay Generator Circuit

The function of this circuit, which is the second block in Figure 1 (a), is the generation of a programmable wide delay range at the output pulse of the proposed CMOS coarse delay line. The Delay Generator circuit's schematic and timing diagram are shown in Figure 2. As can be seen from Figure 2(a), the Delay Generator circuit mainly makes use of a 10-bit synchronous counter, a STOP-Pulse decoder with a network of CMOS transmission gates built inside, and an SR flip-flop. The Start Pulse, TRG_P', is synchronised to count zero of the counter. As shown in Figure 2(b), when TRG_P' goes LOW, the SR flip-flop's output Q changes to HIGH. Hence, the counter's gated clock G.CLK_1 is activated. A custom network comprising 10-bit CMOS transmission gate is designed to function as a switch connecting the synchronous

counter to a Stop-Pulse Decoder circuit. A 10-bit binary word, T_{dC}[9:0], which is programmed at the switch control ports will correspond to the amount of the desired delay. When the clock count is equal to the input digital code value, the Stop-Pulse Decoder detects the count that is equal to the code and generates the first STOP Pulse, STOP_P_D. Consequently, the flip-flop's output Q changes to LOW, the counter's gated clock is deactivated, and the counter is reset. The output of the Delay Generator circuit is P_D which is the complement of Q of the SR-flip-flop. The period of LOW-logic level of P_D is approximately the desired output time delay, T_{dC}.



(a)



(b)

Figure 2. Delay generator circuit: (a) schematic diagram; (b) timing diagram

The minimum achievable coarse delay step, $DS_{C,min}$, at the output of the coarse delay line can be determined from the following equation:

$$DS_{C,min} = \frac{1}{f_{clock}} \tag{1}$$

where f_{clock} refers to the frequency of the counter clock. On the other hand, the maximum achievable coarse delay range, $DR_{C,max}$, at the output can be determined from the following equation:

$$DR_{C,max} = 2^{counter,bit-no.} \times DS_{C,min} \tag{2}$$

According to Equations (1) and (2) and supposing that the 10-bit counter operates with f_{clock} equals to 500MHz, $DS_{C,min}$ is 2ns and $DR_{C,max}$ is approximately 2µs.

The outputs P_D and STOP_P_D of the Delay Generator circuit will serve as the ENABLE and the second START Pulse respectively, for the next circuit block which is Duty-Cycle Controller circuit.

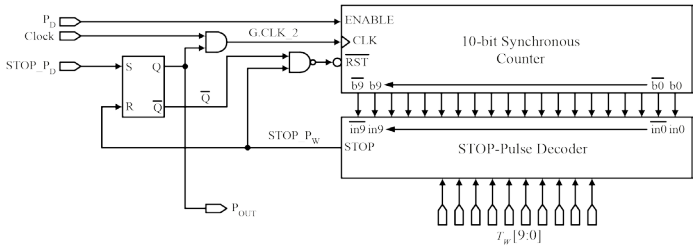
Duty-Cycle Controller Circuit

The function of this circuit, which is the third and last block in Figure 1(a), is the generation of a programmable duty-cycle/pulse-width at the output pulse of the coarse delay line. The Duty-Cycle Controller circuit's schematic and timing diagrams are shown in Figure 3. It is clear from Figure 3(a) that the digital building blocks constructing the Duty-Cycle Controller circuit are similar to that of the Delay Generator circuit. The main difference is in terms of their functionality depending on the input and output of the building blocks of each circuit. As shown in Figure 3(b), when STOP_P_D goes HIGH, the SR flip-flop's output P_{OUT} changes to HIGH.

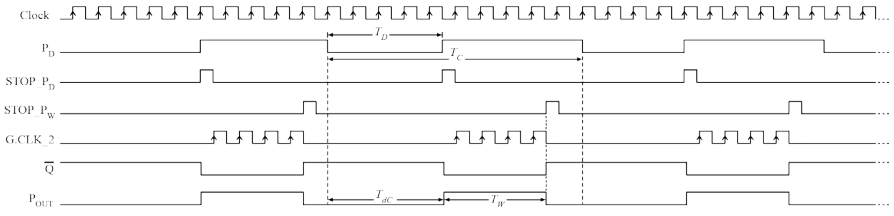
Accordingly, the counter's gated clock G.CLK_2 is activated and the counter starts to count. A 10-bit binary word, T_W[9:0], which is programmed at the control ports of the transmission gate will correspond to the amount of the desired pulse-width. When the clock count is equal to the input digital code value, the Stop-Pulse Decoder detects the count that is equal to the code and generates the second STOP Pulse, STOP_P_W. As a result, the flip-flop's output P_{OUT} changes to LOW, the counter's gated clock is deactivated, and the counter is reset. The period of the HIGH-logic level of P_{OUT} is approximately the desired output pulse-width, T_W.

It is worth mentioning that the maximum achievable periods of the generated time delay, $DR_{C,max}$, and the generated pulse-width, $T_{W,max}$, are restricted to the following relation:

$$DR_{C,max} + T_{W,max} \leq T_C \tag{3}$$



(a)



(b)

Figure 3. Duty-Cycle Controller circuit: (a) schematic diagram; (b) timing diagram

where T_C is the cycle period of the input signal. The condition illustrated in (3) is set to avoid the overlap of the programmable width delayed output pulse with the next cycle of the input pulse.

SIMULATION RESULTS AND DISCUSSION

The proposed CMOS coarse delay line is designed using a 0.13µm CMOS process. The power supply voltage is 1.2V. Referring to Figure 2(a), since the Delay Generator circuit makes use of a 10-bit counter operating with 500MHz clock frequency, the values of the generated $DR_{C,max}$ and $DS_{C,min}$ are approximately 2µs and 2ns respectively. This is illustrated in Figure 4(a).

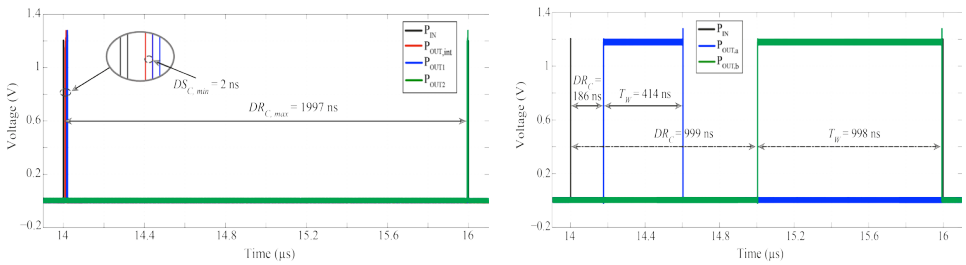


Figure 4. Different output delay and pulse-width values: (a) minimum step and maximum range of the generated coarse delays with a minimum pulse-width value fixed for both delay values; (b) two different cases of generated delay and pulse-width values

In Figure 4(a), the pulse P_{IN} (black) is the input pulse with a width of 2ns and needs to be delayed. On the other hand, pulse P_{OUT1} (blue) is delayed by 2ns which is corresponding to the minimum coarse delay step, $DS_{C,min}$. This is done by setting the digital delay code, T_{dC} [9:0] of the delay generator circuit to [0000-0000-01]. The delay 1997ns of the pulse P_{OUT2} (green) represents the maximum attainable delay, $DR_{C,max}$. This is obtained by setting the digital delay code to [1111-1001-00]. It should be noted that the delay of the red-coloured pulse, P_{OUT}, int, in Figure 4(a) is the intrinsic delay of the CMOS coarse delay line's building circuits. This delay whose value is approximately 5ns is always added to the output delayed pulse. However, this poses no problems because the added intrinsic delay is a constant offset value that can easily be subtracted to obtain the exact desired time delay (Markovic, Tisa, Villa, Tosi, & Zappa, 2013). In Figure 4(b), P_{IN} (black) is again the input pulse to be delayed and has a pulse width of 2ns. P_{OUTa} is output pulse programmed with a delay of 186ns and a pulse width of 414ns. This is obtained by setting the delay code, T_{dC}[9:0], to [0001-0111-01] and the pulse width code, T_W[9:0], to [0011-0011-11]. To demonstrate the pulse width changing capabilities, pulse P_{OUTb} is shown. It is delayed by 999ns and has a pulse width of 998ns. This output is obtained by setting T_{dC}[9:0] to [0111-1100-01] and T_W[9:0] to [0111-1100-11]. Accordingly, the summation of the obtained values of the $DR_{C,max}$ and the $T_{W,max}$ approximately equals to 1999ns which doesn't exceed the cycle period 2000ns of the input pulse T_C. The linearity of the generated coarse time delay, T_{dC}, versus the input digital delay code is also considered and analysed as shown in Figure 5.

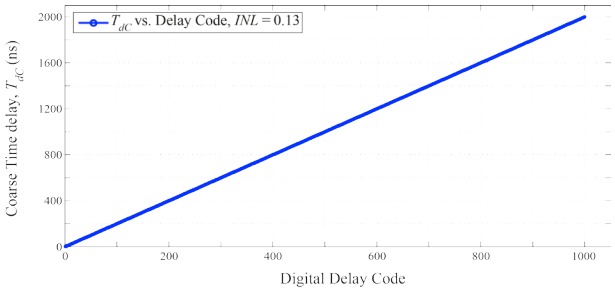
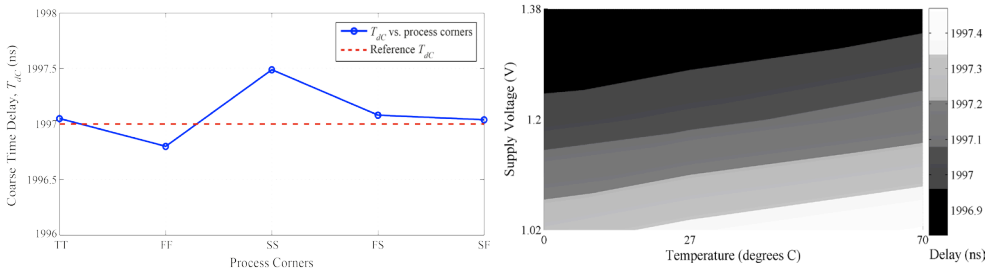


Figure 5. Output coarse time delay, T_{dC}, versus input digital delay code

The x-axis shows the Binary-Coded-Decimal (BCD) value of the programmed delay while the y-axis shows the simulated output coarse delay. Figure 5 clearly shows a linear relationship between the output delay and the input digital delay code as the *INL* value is only 0.13.

Regarding the effects of both process and environmental (PVT) variations on the coarse delay range, Figure 6 can be considered.



(a) (b)

Figure 6. Maximum achievable delay range versus: (a) process corners; (b) temperature and supply voltage variations

It can be seen from Figure 6(a) and (b) that the process as well as supply voltage and temperature variations have a very limited effect on the generated maximum delay range of the coarse delay line.

Figure 7 shows that the layout area required for this circuit is approximately (101 × 142) μm^2. Figure 7 highlights the delay generator circuit and the duty-cycle controller circuit. The circuits are enclosed by two layers of guard rings to prevent the circuits' noise from contaminating other signals if these circuits are used in a mixed signal IC.

A comparison between our coarse delay line and other CMOS implementations is seen in Table 1.

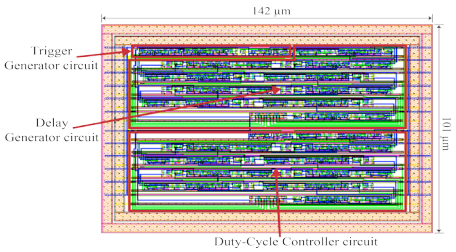


Figure 7. Layout of the proposed CMOS coarse delay line

Table 1
A comparison of this study with other reported CMOS coarse delay lines

Parameter	(Products, 2009)	(Markovic et al., 2013)	(Han, Qiao, & Hei, 2016)	This work
Technology (µm)	0.5	0.35	0.13	0.13
Maximum delay range (ns)	64	160	46	2000
Duty-cycle adjustability	No	No	No	Yes

Table 1 shows the technology used and maximum delay range. A comparison between this work and the most recently published work by (Han et al., 2016) using 0.13µm technology shows that our technique produces the longest delay. This table also shows that only our design has the ability to adjust the delayed output's duty cycle.

CONCLUSION

It can be concluded that an input signal can be delayed for 2µs delay range in steps of 2ns. The duty cycle can also be adjusted in the same range and step provided that the summation of the maximum delay range and the maximum pulse width doesn't exceed the cycle period of the input signal. The small layout area and the low power consumption of the proposed architecture make it suitable for many high-performance SoC circuits.

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