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A Study of Negative Bias Temperature Instability (NBTI) in p-MOSFET Devices

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ABSTRACT

Negative bias temperature instability (NBTI) is a common phenomenon in a p-channel MOSFET device under a negative gate-to-source voltage at a high stress temperature. This paper presents the NBTI characterisation based on different analysis methods and stress conditions on p-MOSFET devices. The atomic hydrogen concentration is probed at interface, Poly-Si and channel of p-MOSFET under study using SILVACO TCAD tool. In addition, the behaviour of the permanent and recoverable component was investigated based on AC stress at different stress conditions using Modelling Interface Generation (MIG) tool. The results show that increases in temperature, negative voltage stress gate and decreases in frequency increase the threshold voltage shift, thus enhancing NBTI degradation.

Keywords: NBTI, temperature, voltage stress gate, frequency, threshold voltage (Vth), AC, DC, recovery

INTRODUCTION

Negative bias temperature instability (NBTI) occurs in p-channel MOSFET that operates with negative gate-to-source voltage at elevated temperature. NBTI contributes to degradation of transistor parameters which are increasing of the threshold voltage, decreasing of transconductance, drain current, channel mobility and subthreshold slope. NBTI not only degrade circuit performance, it can also results in circuit failures (R. Entner, 2014). A gradual shift of threshold voltage (VTH) over time is commonly observed due to the application of voltage stress on the gate, temperature, and the duty cycle for AC only of the stressing voltage under static stress (DC) and dynamic stress (AC) (Mishra, Pandey, & Alam, 2012).

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NBTI mechanism based on R-D model

The model used to define the NBTI mechanism is the rate-diffusion (R-D) model, according to which the electric field was able to break Si–H bonds located at the Silicon-oxide interface. H was released in the substrate where it migrates. The remaining dangling bond Si- (Pb centre) contribute to the threshold voltage degradation. On top of the interface states generation some pre-existing traps located in the bulk of the dielectric (and supposedly nitrogen related), were filled with holes coming from the channel of pMOS. Those traps can be emptied when the stress voltage was removed. This Vth degradation can be recovered over time (Mishra et al., 2012; R. Entner, 2014, Ang, Member, Teo, Ho, & Ng, 2011). Figure 1 shows that released hydrogen diffuses into the gate oxide during stress and returns back to the interface when stress was removed. The active region of the NBTI mechanism was uniformly distributed over the channel according to a one-dimensional problem. Figure 2 depicts that a hole can tunnel to a Si-H bond during inversion of the p-MOSFET and it can take one electron of the covalent bonding away. After that, the hydrogen atom diffuses away with its electron and leaves a positively charged interface trap behind (Entner, 2014).

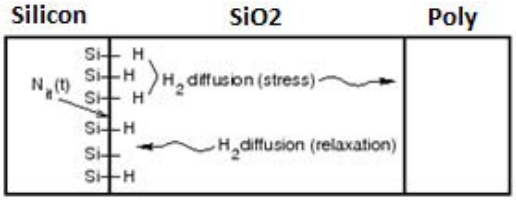

Figure 1. Schematic description of the R-D model (Entner, 2014)

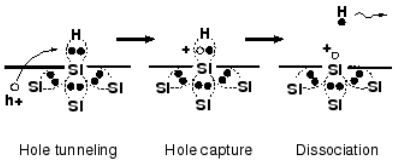

Figure 2. Mechanism for breaking interfacial Si-H bonds by inversion-layer holes (Entner, 2014)

In NBTI, different stress conditions will result in changes in threshold voltage. The methods used in characterizing NBTI degradation causes degradation due to recovery effect to differ (Mishra et al., 2012). Increased defects will lead to shorter device lifetime and device failure. The relationship between the defect shown by the equation below. As the threshold was increased due to the NBTI, the drain current(I_D) and transconductance(g_m) also degraded. A shift in the threshold voltage (ΔV_{TH}) of the PMOS transistor is proportional to the interface trap generation due to NBTI, which can be expressed as

$$\Delta V_{th} = \frac{qN_{it}(t)}{C_{ox}}(1\text{-}m) \quad (1)$$

Where m represents equivalent V_T shifts due to mobility degradation (or model parameter), q is the electronic charge, and Nit (t) is the interface trap generation, which is the most important factor in evaluating performance degradation due to NBTI for R-D model (Mishra et al., 2012).

Generation and Recovery of Interface Trap

Based on the pre-existing interface traps and creation of the new interface states, there were two components of NBTI which were permanent and temporary as shown in Figure 3 (Mishra et al., 2012). Permanent NBTI was known as non-recoverable because of the new interface trap generation. Meanwhile, temporary NBTI was known as recoverable because of some pre-existing traps present in the gate oxide was filled with holes from the PMOS channel and the hole can be emptied when the stress voltage was removed (Mishra et al., 2012). The component that effect most of the increasing of threshold voltage was mainly due to the permanent NBTI rather than temporary which partly effect threshold voltage (Mishra et al., 2012).

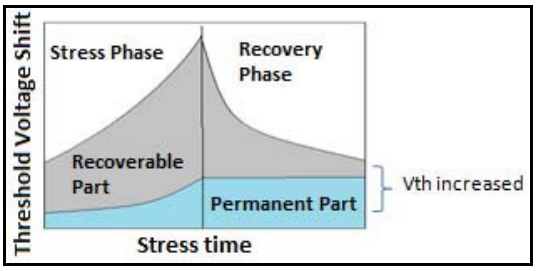

Figure 3. Temporary and permanent phase of NBTI (Mishra et al., 2012)

An early hypothesis was made based on the review paper by Mahapatra (Mahapatra et al., 2013), in negative stress bias (V_G) results in increasing of NBTI phenomenon although the magnitude depends on gate oxide field (E_{ox}). NBTI phenomena shown to be a temperature dependant where it increases at elevated temperature based on Arrhenius law. Gate oxide field, temperature and stress time can be summarized to be related in increasing of NBTI phenomena by a simple analytic formula (Franco, 2014):

$$\Delta V_{th} \approx \left(-\frac{E_A}{k_B T}\right)\left(\frac{|V_G - V_{tho}|}{t_{ox}}\right)^{\gamma} t_{stress}^{n} \quad (2)$$

Where E_A is an apparent activation energy, k_B is the Boltzmann constant and T is the stress temperature.

In this paper, we probe atomic hydrogen concentration at different location of p-MOSFET device interface, Poly-Si and channel using SILVACO TCAD. The threshold voltage shift of p-MOSFET based on different stress condition in DC and AC analysis were analysed and the behaviour of the permanent and recoverable component of p-MOSFET subject to AC stress we studied.

METHODOLOGY

In this project, SILVACO TCAD and Modelling Generation (MIG) were the simulation tools used to study the NBTI phenomenon. Figure 4 shows a process flow of creating device structure and characterization process using ATHENA and ATLAS respectively. The atomic hydrogen

concentration was probed at interface, Poly-Si and channel of p-MOSFET as to observe the generation of interface trap at three different location in the MOSFET device (Coulombs, 2010). In this work, a conventional SiO2 p-MOSFET device with gate length of 1µm was created as shown in Figure 5.

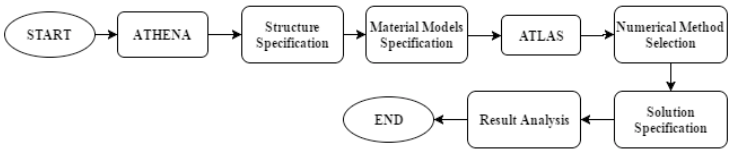

Figure 4. The process design flow in SILVACO TCAD

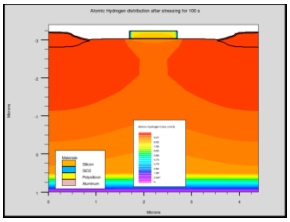

Figure 5. A submicron device structure of p-MOSFET

The MIG was a simulation tool used to estimate the change in the interface trap (ΔN_{IT}), hence threshold voltage shift (ΔV^{T}), resulting from NBTI phenomena, based on the voltage, temperature and stress conditions given. It can be used to mimic the experimental condition by indicating the points where ΔV_T measurement has to be taken, including the effect of delay (due to ΔV_T measurement time required by the setup). Finally, based on the measured ΔV_T under DC (continuous stress) condition, projection of lifetime, t_{life} (the time at which the device will degrade up to a certain value of ΔV_T) can be made at both DC and AC (periodic stress, having duty cycle of 50%) (Islam, n.d.).

EXPERIMENTAL RESULTS

Effect of Different Probing Location based on Different Stress Temperature and Stress Voltage

A stress was applied to this submicron device by varying the voltage stress and temperature. Based on the result of the simulation, the hydrogen concentration was studied at three different location: centre of the interface, Poly-Si gate contact and Si channel (Coulombs, 2010). The atomic hydrogen concentration was observed as to understand the breaking of Si-H bond during the stress phase and hydrogen passivation during the recovery phase (Mishra et al., 2012).

Temperature ranging from 300K to 420K was applied with same voltage stress on the gate oxide of -2V. The applied temperatures were within the range of 100°C to 150°C, within which significant NBTI degradation was observed (Hussin, Soin, Bukhori, Abdul Wahab, & Shahabuddin, 2014). A total dangling bond density of 1 x 10 cm^{-2} was assumed (initially passivated 100%) (Coulombs, 2010). However, the result shown that the total dangling bond was not passivated at 100%. This was due to the submicron device structure does not completely created properly in SILVACO ATHENA.

Based on Figure 6 – Figure 8, the atomic hydrogen concentration at 420K shows higher concentration than temperature at 398K and 300K. This was because under a high temperature

the hydrogen diffuses much more faster which was why at temperature 420K has higher concentration that 398K and 420K. The hydrogen diffuse more in centre of interface than in Poly-Si contact and Si contact due to the electric field break Si-H bond at the centre of the interface located at the Silicon-oxide interface (Entner, 2014).

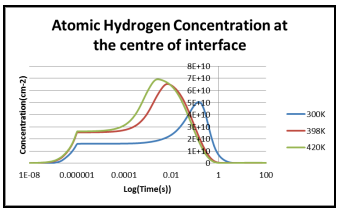

Figure 6. Atomic hydrogen concentration at the centre of the Interface

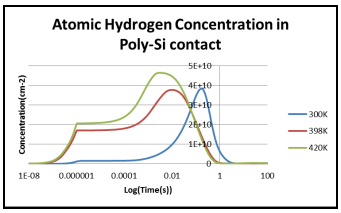

Figure 7. Atomic hydrogen concentration in Poly-Si contact

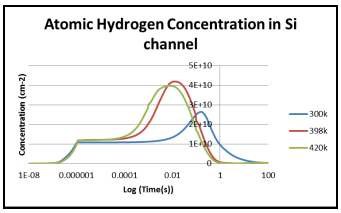

Figure 8. Atomic hydrogen concentration in Si channel

Next, negative voltage stress on the gate oxide from range -1.5V to -2.5V were applied. This time the temperature were set to constant temperature of 398K. The collected data were used to fit the model parameters for NBTI simulation (Wittmann et al., 2005). The applied stress voltages, VS, were varied between -1.2 V and -2.52 V such that the oxide electric field (E) was maintained within the range of 6 MV cm^{-1} to 11 MV cm^{-1} in both p-MOSFETs with different Equivalent Oxide Thickness (EOT), thus replicating stress conditions in real-life experiments (Hussin et al., 2014). The expected total dangling bond was also the same during temperature stress: 1 x 10^{12} cm^{-2}.

Figure 9 – Figure 11 show the atomic hydrogen concentration at three different location. The concentration at voltage stress of -2.5V was higher than voltage stress of -1.5V and -2V. The higher the temperature and voltage stress will result in higher hydrogen passivation (Mishra et al., 2012). Thus, generate more interface trap which later result in increasing the threshold voltage (V_{TH}). Increasing in threshold voltage (V_{TH}) will result the NBTI degradation.

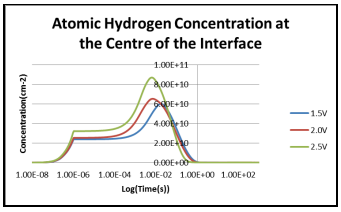

Figure 9. Atomic hydrogen concentration at the centre of the Interface

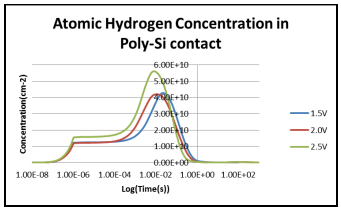

Figure 10. Atomic hydrogen concentration in Poly-Si contact

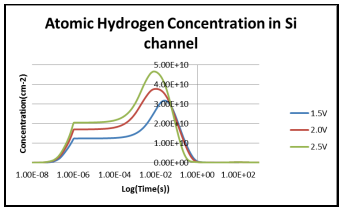

Figure 11. Atomic hydrogen concentration in Si channel

Effect of Different Stress Condition based on AC Measurement

In AC analysis, similar range of temperature stress and voltage stress used in DC analysis will be applied. In addition, a frequency from a range of 0.001Hz to 0.01Hz as to account for AC measurement was applied. The permanent and recovery component plays an important role to study the NBTI characterization. The recovery mechanism can be observed when a device was subject to a train of stressing pulses which was known as AC stress (Mishra et al., 2012).

During the first phase of the clock cycle, V_{th} increases due to the stress applied, and then it decreases again in the second half of the cycle when the stress was removed as shown in the Figure 12 below (Mishra et al., 2012). As shown in the figure, a CMOS inverter was drawn and when the V_g i.e. input gate voltage is zero (i.e. V_{gs}= -V_{DD}), the PMOS will be in the stress phase and when V_g is V_{DD} (i.e. Vgs= 0) then PMOS will be in relaxation phase as shown (Mishra et al., 2012). It is important to understand the stress and recovery phenomenon in p-MOSFET devices as the operation of CMOS inverter can significantly affect by the reliability issues specifically the NBTI occurrence in a p-MOSFET devices.

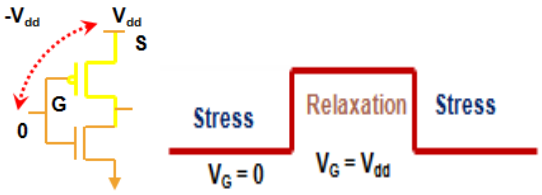

Figure 12. Pulse showing stress and relaxation phase of a PMOS (Mishra et al., 2012)

Figure 13 shows the permanent and recoverable component of the p-MOSFET device under stress of temperature at 125°C, voltage stress gate at -2.0V and frequency at 0.001Hz. The permanent component, ΔV_t^s was created as the new interface trap generation when the device was put under stress meanwhile the recovery component, ΔV_t^r was obtained when some pre-existing traps present in the gate oxide was filled with holes from the PMOS channel and the hole can be emptied when the stress voltage was removed (Hussin et al., 2014). The device was stressed and relaxed until 5000s in 5 cycle. The threshold voltage (V_{TH}) increase slightly for each cycle at the end of applied stress and recovery.

Effect of Different Stress Condition based on Permanent and Recoverable Component

Figure 14 and 15 show the permanent and recoverable threshold voltage (VTH) under three different stress condition: temperature (range from 75°C to 150°C), voltage stress gate (range from -1.6V to -2.3V) and frequency (range 0.001Hz to 0.01Hz). The permanent component in Figure 14 can be obtained by subtracting the threshold voltage (V_{TH}) at the end of recovery with the threshold voltage (V_{TH}) at the beginning of stress (Hussin et al., 2014). Same with the permanent component, the recovery component in Figure 15 also can be obtained by subtracting the V_{TH} at the end of recovery and V_{TH} at the beginning of the recovery (Hussin et al., 2014).

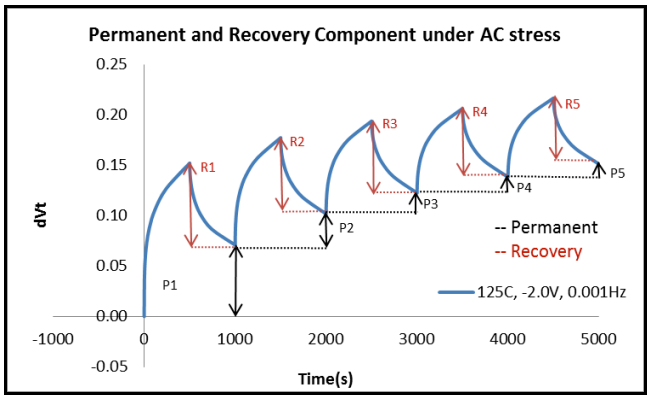

Figure 13. Permanent and Recoverable component at different temperature under AC stress

The permanent and recoverable shift V_{TH} decreases as the cycle increases. This result was consistent with the self-limiting recovery perspective, where in the recovery is dependent on the number of stress cycles (Hussin et al., 2014). This degradation mechanism, in which a reduction in the recovery is observed, can be explained by the influence of increasing stress recovery cycles that can contribute to greater structural relaxation; consequently, the oxide network was distorted and the hole traps cannot be recovered, thus being transformed into a more permanent form (Hussin et al., 2014). The graph was obtained using the same method in paper (Ang et al., 2011; Grasser et al., 2010; Hussin et al., 2014; Jia et al., 2013).

The threshold voltage shift increases as the frequency decreases. This is due to at high frequency, there was an asymmetry of the delays between dissociation and annealing (Entner, 2014). It can be speculated that a short delay exists between the availability of holes and their capture by Si-H bonds. It can be assumed that the slower starting of the dissociation process was responsible for the reduced threshold shift in the higher frequency (Entner, 2014).

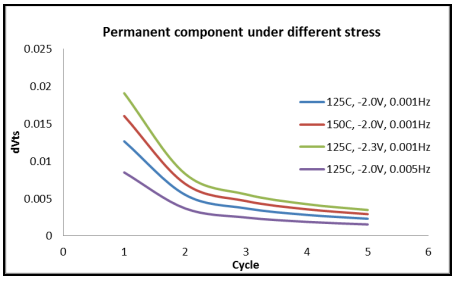

Figure 14. Permanent component of different stress under AC stress

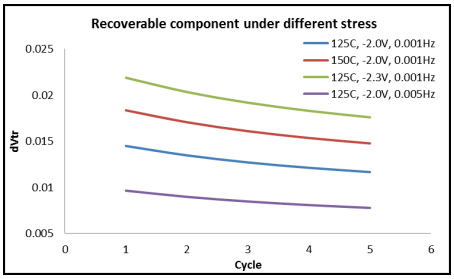

Figure 15. Recoverable component of different stress under AC stress

DISCUSSION

Concentration of atomic hydrogen on three different locations on p-MOSFET were influenced by temperature and negative voltage stress (V_G). Higher temperature results in a higher probability of hydrogen diffusion in the centre of the interface to gate oxide from the breaking of Si-H bond due to the electric field during the stress phase. The process of breaking the Si-H bond becomes much faster at elevated temperature until at its peak of stress time before it diffuses back into SiO^2 to recombine back into Si-H bond during the recovery phase. The negative voltage stress (V_G) with a magnitude of the gate oxide field (E_{OX}) creates the electric field which is capable of breaking the Si-H bonds. As the V_G increases, the electric field becomes much stronger, which causes more Si-H bonds to break to produce a hydrogen atom. As the atomic hydrogen concentration increases, the V_{TH} shift also increases, which lead to NBTI degradation effects. In DC stress, the threshold voltage shift (V_{TH}) increases with the applied stress time. For AC stress, there are stress phase and the recovery phase in each cycle in a specific period of time. The stress time and recovery time, reduce for the next cycle. This result to less permanent and recovery component in the next cycle. The permanent and recoverable component decreases over time in each cycle due to less stress and recovery time for each cycle.

Temperature and negative voltage stress (with a magnitude of oxide field) are well-known NBTI dependence. Therefore, it is very crucial to determine the range of applied stress voltage and temperature during the NBTI characterization process to reduce the possibility of other defect mechanisms such as Time Dependent Dielectric Breakdown (TDDB) and hot carrier injection (HCI) occur. Higher frequency also reduces NBTI degradation in AC analysis. In view of the recovery process being significant in reducing the NBTI effects, to ensure no recovery contribution during the stress-measure-stress characterization process, other techniques such as fast and ultra-fast on-the-fly (OTF) techniques can be used as this method do not suffer from recovery artefacts and are suitable for measuring degradation from short to long t-stress (Mahapatra et al., 2013).

CONCLUSION

This paper presents the NBTI degradation phenomenon for DC and AC analysis, which the underlying mechanisms based on R-D model. The Silvaco TCAD tool was used as to understand the behaviour of interface trap concentration. Using the MIG tool, higher temperature and negative voltage stress gate well as lower frequency results in higher threshold voltage shift The permanent and recoverable threshold voltage shift decreases as the cycle increases during AC measurement. A Two Stage the underlying mechanism includes the pre-existing effect together with the interface trap can be used in future work as to enhance the understanding of NBTI degradation in p-MOSFET devices with different technologies such as high-k devices and advanced FinFET technology with regard to the recoverable component issues.

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