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RF CMOS Switch Design Methodologies for Multiband Transceiver Applications

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ABSTRACT

Multimode multiband connectivity has become a de-facto requirement for smartphones with 3G WCDMA/4G LTE applications. In transceivers, multiband operation is achieved by selecting an output from two or more signal path targeting for a specific frequency range in parallel or by using switched capacitor/inductor. In this paper, design methodology of 280nm CMOS switch is presented. Design optimization of RF CMOS switch is presented which is deciding proper selection of CMOS transistor parameters and switch size as per external circuit parameters. The CMOS switch of a 5-transistor stack with W/L=1200µm/280nm provides insertion loss < 0.6dB and isolation loss >14dB. The switches designed when implemented in a multiband power amplifier (PA) exhibits 36dB gain at 1900MHz high-band and 34.5dB gain at 900MHz low-band with 27.5dBm peak power at both bands. The switch design methodologies presented in this paper should be of use in designing various blocks in emerging multiband transceiver applications.

Keywords: CMOS RF switch, insertion loss, isolation loss, multiband power amplifier, Long Term Evolution (LTE)

INTRODUCTION

Wireless communication is evolving at a very fast rate and the smartphone devices need to be able to connect to more than one band of frequency (Moon, 2015; Cheng & Young, 2011) in order to support global roaming facilities. Transformer matching or LC matching is usually used in PA design at LTE operational frequencies. In order to achieve matching at a particular band frequency band,

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the capacitor that is parallel to the transformer inductor or the capacitor in the LC matching network is tuned. For example, a tunable multiband PA was demonstrated by Ali et al. (2010) using BST (barium-strontium-titanate) varactor based tuning at frequencies from 1.7GHz to 2.2GHz; a multiband PA by Neo et al. (2006) using silicon-on-glass varactor diode for tuning was realized; a multiband PA using four number of MEMS switches was realised by Fukuda et al. (2006); and Kang et al. (2013) reported an MB PA that uses PIN diode switches. A multiband PA in the GaAs heterojunction-bipolar transistor (HBT) is presented by Lee et al. (2015), in which the input and output matching networks are tuned to achieve multiband operation.

In the above works, BST and MEMS-based tuning cannot be realised in CMOS process and PIN diode is not available in most of the standard CMOS PDK. Therefore, transformer matching with switches or LC matching with switches is used in the CMOS based PA design. However, the parasitic of the CMOS transistor switch degrades the gain and linearity of the PA, and hence optimum design of the switch is very essential. There are a few works reported on CMOS switch design (Yeh et al., 2006; Min & Rebeiz, 2007; Li et al., 2008) for transmit/receive (T/R) application associated with connecting antenna to the transmit and receive path. However, design of CMOS switches for individual multiband RF modules that is efficient is needed.

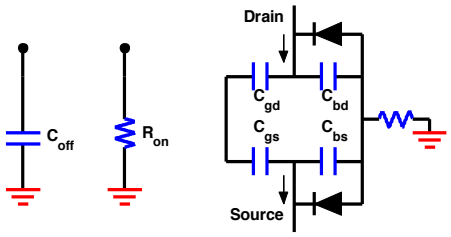
In this paper, the design methodologies of CMOS switch for minimum insertion and maximum isolation losses is presented. The designed switches are then integrated in a multiband PA design and its performance examined.

METHODOLOGY

CMOS Switch Design

In general, a transistor can be considered as a parasitic capacitor when it is in the OFF state and as a resistor when it is in the ON state as shown in Figure 1. The parasitic diode between the bulk and drain terminals is forward-biased during the negative half cycle of the ac signal; and similarly, the parasitic diode between the bulk and source terminals is forward-biased during the positive half cycle of the ac signal. Thus, in the OFF state of the transistor, the conduction of current through the parasitic diodes greatly affects the output power and linearity when used in PA application. Therefore, in this design, the bulk of the transistor is connected to the substrate (ground) through a resistor value of 10kΩ to control leakage current. In addition, the transistors should be stacked (let the number of series connected transistor be defined as stack length) in such a way that the voltage distributed across the parasitic capacitors is less than the "turn-on" voltage of the diodes. Moreover, when the transistor is ON, its resistance R_{on} should be as small as possible to achieve high gain and high output power. Therefore, an optimum design of CMOS switch becomes essential.

Investigations of the transistor ON state resistance and OFF state capacitance in the Silterra (Kedah, Kulim, Malaysia) 280nm CMOS transistor is taken here for the optimum switch design. Transient analysis was performed using Cadence simulation and the transistor ON state resistance calculated using Ohm's law (i.e. V_{DS}/I_{DS}). To determine the OFF state

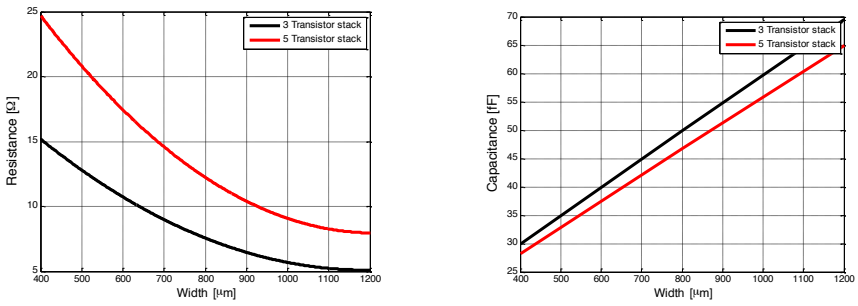


(a) (b)

Figure 1. CMOS transistor-based switch implementation (a) transistor equivalent in the OFF and ON state (b) simplified equivalent model of a parasitic transistor

capacitance, transient analysis was performed and the power consumed by the switch was determined using the *integ* function available in the Cadence Spectre calculator, and then the capacitance estimated from the relation $P=C\times V^2\times f$.

Figure 2(a) shows the ON state resistance of the switch with respect to the changes in the width of the transistor and its respective stack length; from which it is understood that increasing the transistor width will decrease the ON state resistance of the transistor. As such, if the CMOS switch in the circuit requires handling high current then the switch design should opt for larger transistor size. Moreover, as seen from the Figure 2(a), the resistance increases with higher stack length because the resistance of each transistor that is being stacked in series will be added to the total ON state resistance.



(a) (b)

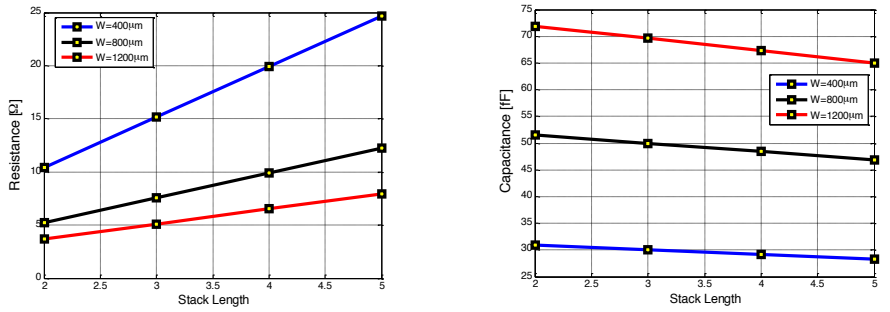
Figure 2. (a) ON state resistance, and (b) OFF state capacitance of the switch versus transistor width

On the other hand, Figure 2(b) shows the OFF state capacitance of the switch with respect to transistor width and transistor stack length; from which it is understood that increasing the transistor width will increase the transistor OFF state capacitance linearly. As such, if the external circuit capacitance value is high then the switch design should opt for smaller size transistor provided current through the switch is not constrained. If the current is constrained to a certain value, then the design should opt for increasing the stack length. Moreover, as seen

from the Figure 2(b), the capacitance decreases when the stack length increases, because of the reduced series capacitance of the transistors in the stack.

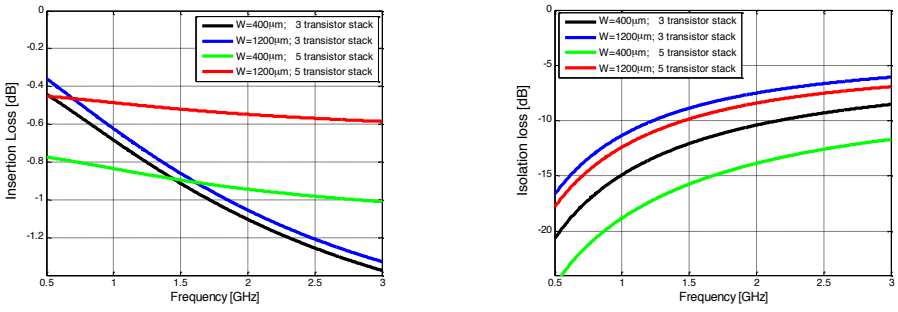
Figure 3(a) shows the ON state resistance of the switch with respect to the transistor stack length and the transistor width; from which it is clear, as expected, that increasing the stack length increases the transistor ON state resistance. Therefore, when the switch is designed to handle high voltage, then high stack length should be used so as to distribute the voltage across the parasitic diodes to be less than its 'turn-on' voltage. For 280nm CMOS transistor, the V_{DS} of less than 3V will keep the diodes 'turn-off'. Therefore, for every V_{DS} increment by 3V the stack length should be increased by one transistor.

Similarly, on the other hand, Figure 3(b) shows the OFF state capacitance of the switch with respect to the transistor stack length and the transistor width. The capacitance decreases rather slowly for an increase in stack length but rapidly decreases for the decrease in transistor width. To have a good isolation in the OFF state, the reactance of switch parasitic capacitance should be higher than the external circuit capacitance. That is $X_{Coff} >> X_C$ or $C_{off} << C$; where C is the external circuit capacitance and C_{off} is the switch OFF state parasitic capacitance.



(a) (b)

Figure 3. (a) ON state resistance, and (b) OFF state capacitance of the switch versus transistor stack length



(a) (b)

Figure 4. (a) Insertion loss (when the transistor in ON), and (b) Isolation loss (when the transistor OFF) of the switch against frequency

Figure 4(a) shows the insertion loss of the switch as a function of frequency. For a good switch the insertion loss has to be a minimum. It can be seen from the figure that the insertion loss increases with frequency. The loss can be minimised by increasing the transistor width for a fixed stack length; and/or by increasing the stack length for a fixed transistor width. Insertion loss of 0.4-0.6dB is nominal in a standard CMOS process (Kidwai et al., 2009). A 5-transistor stack with W=1200µm in Silterra CMOS offers a loss of ~0.5dB at the LTE operational band of frequencies, as such, it is found to be the optimum choice for the switch design. Similarly, Figure 4(b) shows the isolation loss of the switch as a function of frequency. For a good switch the isolation loss has to be a maximum. It can be seen from the figure; the isolation loss decreases with frequency. The loss can be maximized by decreasing the transistor width for a fixed stack length; and/or by increasing the stack length for a fixed transistor width.

Based on the above investigation, the switch design analysis can be summarised as in Figure 5. The transistor width is directly proportional to the current requirement of the switch and inversely proportional with the external capacitance (Cs) that the switch should be connected to. Therefore, the choice of transistor width depends on the right balance between current through the switch and the external capacitance value. When the requirement of current through the switch is fixed, then one should consider increase or decrease the stack length based on the external capacitance. Similarly, for a fixed external capacitor value we should increase or decrease the transistor width based on the requirement of current through the switch. The stack length should also increase with external node voltage (Vs) as shown in Figure 5. Thus, the correct choice of transistor width and stack length will provide minimum loss during ON state and maximum (isolation) impedance in OFF state leading to optimum circuit performance.

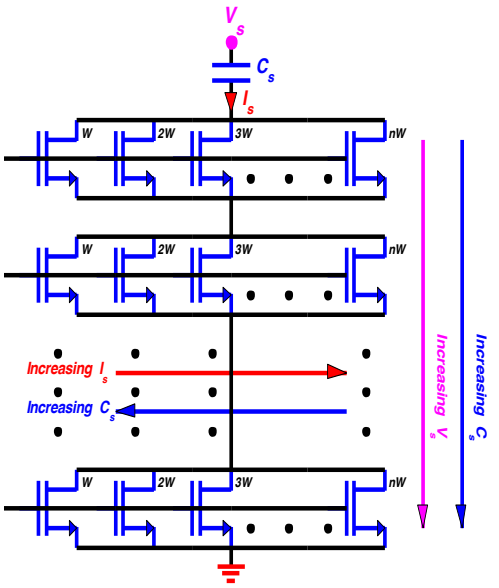


Figure 5. Switch implementation using stacked transistor array (shows how the transistor width and stack length changes with changes in circuit voltage, current and capacitor value)

Multiband PA Design using CMOS Switch

To evaluate the performance of the CMOS switch designed as per methodologies explained above, a multiband PA (Thangasamy et al., 2016) is designed as shown in Figure 6. Supply voltage of 3.3V is applied for the power stage and 1.2V for the driver stage. Switches S1, S2 and S3 are the CMOS switches designed to switch the PA operation from one operating band in to another band. The switches connect the capacitors C11, C31 and C51 in parallel with fixed capacitors C1, C3 and C5, respectively and thus the PA operating band is shifted. The schematic of switches S1, S2 and S3 is shown in Figure 7; whereby S1 is designed with two transistor stack with W/L= (10µm×20)/280nm for each transistor, S2 is three transistor stack with size of each transistor W/L= (10µm×50)/280nm, and the switch S3 is designed with 5 transistor stack with size of each transistor W/L=(10µm×60×2)/280nm.

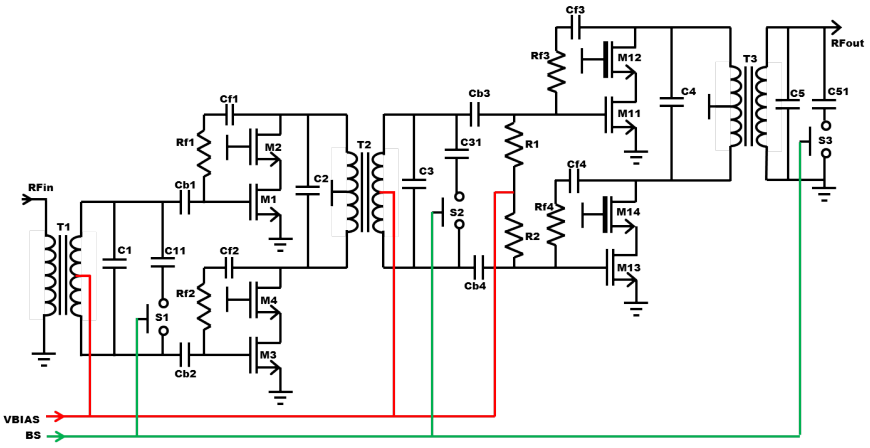


Figure 6. Circuit schematic of multiband PA with CMOS Switch

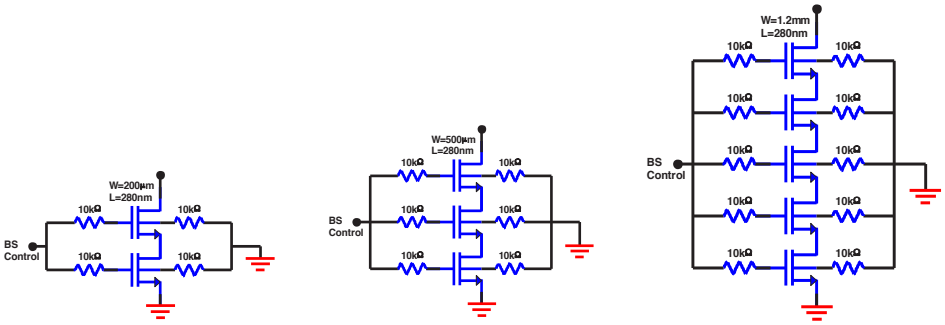
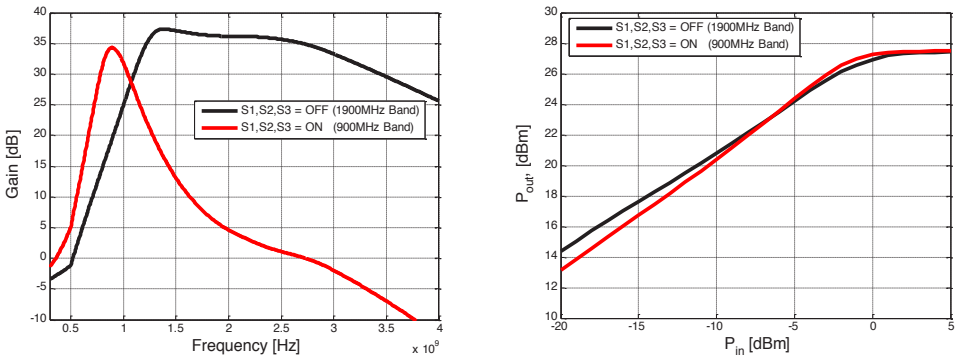


Figure 7. Schematic of (a) switch S1 with two transistor stack and W/L=200µm/280nm (b) switch S2 with three transistor stack and W/L=500µm/280nm (c) switch S3 with five transistor stack and W/L=1.2mm/280nm

Here it can be seen that the switch S1 is used at the input stage, S2 is used at the intermediate stage, and S3 is used at the output stage of the PA. During simulation, at peak output power, the voltage across S1 swing around 1V, voltage across S2 swing around 4V, and voltage across S3 swing around 10V. As such, the transistor stack size is proportionally increased as shown in Figure 7. Moreover, at peak output power, the current through S1 is about 10mA, current through S2 is about 70mA, and that through S3 is about 150mA; as such, the transistor W/L ratio is proportionally increased for S1 through S3 as shown in Figure 7.

RESULTS AND DISCUSSION

The performance of the multiband PA with integrated switches has been evaluated and the simulated gain is shown in Figure 8(a). When the switches S1, S2 and S3 are OFF then the PA responds for 1.2GHz to 2.7GHz frequency band; and when the switches are ON the PA operation shifts to 820MHz to 920MHz band. Between the two gains there is a difference of nearly 1.5dB which is due to the insertion losses of the three switches. Similarly, the achieved P_{out} versus P_{in} performance of the multiband PA with integrated switches is shown in Figure 8(b).



(a) (b)

Figure 8. (a) S-parameter results, and (b) Pout versus Pin characteristics of multiband PA

When the switches S1, S2 and S3 are OFF then the PA has P1dB of 26dBm with maximum power at 27.5dBm; and when the switches are ON the PA has P1dB of 27dBm with maximum power at 27.5dBm. Between the powers there is a difference of nearly 1dBm in the low power region which is due to loss in the switch; however, in the high-power region these two powers are almost same. Thus, the optimum design of CMOS switch enables the multiband PA to deliver optimum power output and optimum gain in either band of operations.

CONCLUSION

Following the growing need for multiband RF modules efficient design of CMOS switches has become important. In this paper, we presented the design methodologies of CMOS switches in view of getting minimum insertion loss and maximum isolation loss as need for the switches in multiband RF module design applications. The switches designed on integration into a

multiband power amplifier exhibits good gain and output power performance both in ON state and OFF state of the switch. The switch design methodologies presented here should be useful in CMOS based multiband circuitry applications.

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